REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

Claims 1-13 are pending in the present application before this amendment. By the present amendment, claims 1-13 have been cancelled without prejudice, and claims 14-15 have been added. No new matter has been added.

In the Office Action, claims 1-5, 7-8, 10, and 12-13 stand as being anticipated by "A Low-Noise CMOS Prescaler for 900 MHz to 1.9 Ghz Wireless Applications", IEEE 1999 Custom Integrated Circuits Conference, pp. 597-600 (Chang). The "et al." suffix in a reference name is omitted in this paper.

Applicant respectfully **disagrees**.

Applicant respectfully asserts that Chang's prescaler does not teach or suggest the invention of claims 1-13, and thus the cancellation of claims 1-13 herein is not motivated to overcome or get around the grounds of present rejection. Claims 14-15 are presented herein for better scope of coverage.

The presently claimed invention teaches that the divider in a DLL circuit of a memory device can divide the input clock 1/8 or 1/16 according to the **operational condition** of the memory device, i.e., whether the memory device is in a power down mode or not, to reduce power consumption. Chang does not teach this claimed limitation.

(1) The divider of the presently claimed invention is used in a **memory device**, as this is clearly recited in claims 14-15, whereas the prescaler of Chang is not utilized in a memory device, but in various wireless communication applications.

(2) Because the divider of the presently claimed invention is used in a DLL circuit in a memory device, the output of the divider is changed according to the **operational mode of the memory device** in order to reduce power loss. Chang is

incapable of carrying out this claimed feature due to structural and design differences because Chang's prescaler is not adapted for application in a memory device.

At least on these grounds alone, Chang does not teach or disclose claims 14-15.

Further, Applicant respectfully points out that the examiner's understanding of the "divide-by-128/129 and 64/65 dual-modulus prescaler" as shown in Figure 1 of Chang is **not correct** to allege that Chang's **prescaler** teaches the claimed clock divider of claims 14-15 (an example of which circuit is shown in FIG. 4 of the present application).

Chang's prescaler in Figure 1 teaches three DFFs, five toggle flip-flops, and several gates. A synchronous divide-by-4/5 counter is formed by the DDFs and the NAND gates. The chain of five toggle flip-flops form a synchronous divide-by-32 counter. Depending on the logic value at "node" in Figure 1 of Chang, the division ratio of the synchronous divide-by-4/5 counter will be either 4 (e.g., "node" = 0) or 5 (e.g., "node" = 1). The signal "s" is used to select the dual-modulus division ratio 128/129 or 64/65. More specifically, the prescaler of Figure 1 of Chang will be:

(1) either a divide-by-64 divider or a divide-by-65 divider depending on the signal level of the "node" whenever the signal level of "s" is at one level (for example, high); or

(2) either a divide-by-128 divider or a divide-by-129 divider depending on the signal level of the "node" whenever the signal level of "s" is at another level (for example, low).

This is the typical and known characteristics of a divide-by-128/129 and 64/65 dual-modulus prescaler that is utilized in Chang.

First, Chang's divide-by-128/129 and 64/65 dual-modulus prescaler by definition requires two control signals "node" and "s" to select from 128, 129, 64, or 65 dividing ratios. Chang follows this design as it describes in page 571:

> "A. Prescaler Topology
> "... The core circuit consists of a synchronous divide-by-4/5 divider followed by an asynchronous divide-by-16/32 divider. Control signals of "S" and "Mode" were used to set the division ratio to divide by -64, -65, -128, or -129 operation."

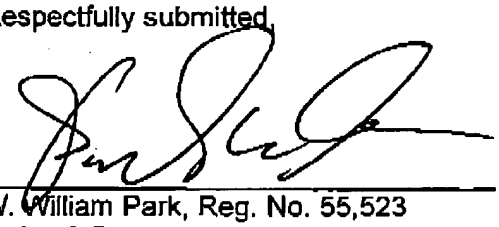
Further, according to the circuit of divide-by-128/129 and 64/65 dual-modulus prescaler as shown in Figure 1 of Chang, divide by 64 is not what is outputted by the "x11" DFF and the divide by 128 is not what is outputted by the "x12" DFF.

Second, Chang's divide-by-128/129 and 64/65 dual-modulus prescaler does not allow such flexibility of adding or subtracting the number of flip-flops to set the dividing ratio. Rather, Chang's divide-by-128/129 and 64/65 dual-modulus prescaler by design utilizes the two stage structure as shown in Figure 1 with specific circuit components.

For the reasons set forth above, Applicant respectfully submits that claims 14-15, now pending in this application, are in condition for allowance over the cited references. This amendment is considered to be responsive to all points raised in the Office Action. Applicant does not believe that the present amendment to claim 1 is rather clarifying in nature and doe not present new grounds for search. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an issuance of a Notice of Allowance.

Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,



Dated: August 12, 2005

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